A MONOLITHIC GaAs DC TO 2 GHz FEEDBACK AMPLIFIER

W.C. Petersen, A.K. Gupta, D.R. Decker

Rockwell International
Microelectronics Research and Development Center
Thousand Oaks, CA 91360

ABSTRACT

Resistive feedback in low frequency FET amplifiers is an attractive method of simultaneously attaining gain flatness and excellent input/output VSWR over wide bandwidths. Combined with simple matching circuitry, the feedback approach allows the design of general purpose utility amplifiers requiring much less chip area than when conventional matching techniques are used. The 1.5 by 1.5 millimeter chip described in this paper provides 10 dB ± 1 dB gain, excellent input and output VSWR, and saturated output power in excess of +20 dBm from below 5 MHz to 2 GHz. The noise figure is approximately 2 dB when biased for minimum noise, with an associated gain of 9 dB.

INTRODUCTION

Negative feedback amplifiers have found wide acceptance in the marketplace for low frequency bipolar transistor designs, and have recently been introduced as the first commercially available GaAs monolithic microwave integrated circuit.[1] Continuing work on this fruitful design technique will lead to improved amplifier performance on smaller chips while incorporating more bias and signal processing circuitry on the chip. The low frequency FET feedback amplifier described in this paper provides resistive bias isolation for ease of use, but also allows the direct application of drain bias for efficiency sensitive applications. A resistively isolated gate bias line allows operation of the FET under either low noise or high power bias conditions for further versatility.

THEORY

The design of resistive feedback FET amplifiers is based on the near-ideal voltage controlled current source characteristics of a microwave GaAs FET operated at low frequencies. Application of series and shunt resistive feedback as shown in Figure 1 provides simultaneous input and output match while maintaining flat gain from DC to a frequency determined by the parasitic elements of the FET and circuit elements. For an ideal FET with transconductance, g_m, gain of the circuit shown in Figure 1 is given by:

$$G_T = \frac{2 Z_o(1 + g_m R_s) - 2 g_m Z_o R_p}{g_m Z_o^2 + 2 Z_o(1 + g_m R_s) + R_p(1 + g_m R_s)} \quad ,$$

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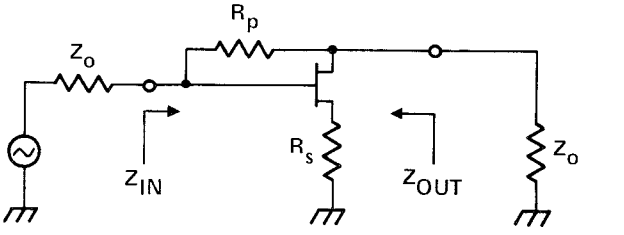

Figure 1 Series and shunt resistance feedback applied to an ideal FET.

while input and output impedance are given by:

$$Z_{in} = Z_{out} = \frac{(R_p + Z_o)(1 + g_m R_s)}{1 + g_m(R_s + Z_o)} \quad ,$$

where Z_o is the system impedance. Under perfect match conditions,

$$Z_{in} = Z_{out} = Z_o \quad ,$$

which implies that

$$R_p = \frac{g_m Z_o^2}{1 + g_m R_s} \text{ and } G_T = \frac{Z_o - R_p}{Z_o} \quad .$$

In order to have amplification, it is necessary that $|G_T| > 1$ which, under matched conditions reduces to $g_m > 2/(Z_o - 2R_s)$ for positive g_m, Z_o, and R_s. Since g_m is proportional to FET width, which must be kept at a minimum, $R_s = 0$ should be selected. With $R_s = 0$ and perfect input and output match the well known formula:

$$R_p = g_m Z_o^2 \text{ and } G_T = 1 - g_m Z_o$$

are obtained. However, it is often advantageous to allow a slight VSWR degradation in order to increase amplifier gain. Assuming $R_s = 0$ and assuming an input and output VSWR of K:1 are acceptable, selecting

$$R_p = K Z_o (1 + g_m Z_o) - Z_o$$

will yield the allowed VSWR and a gain of:

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$$G_T = \frac{2(1 - Kg_m Z_o)}{1 + K} \quad .$$

As an example, if g_m = 80 mS, under matched conditions R_p would be 200 ohms resulting in a gain of 9.54 dB, but if a 1.5 to 1 VSWR is acceptable, R_p becomes 325 ohms and gain is increased to 12.04 dB. However, additional trade-offs are also inherent in this gain enhancement technique. Reducing the amount of negative feedback applied allows the effects of parasitic elements to become apparent at lower frequencies, thus reducing amplifier bandwidth. The dominant parasitic elements are the FET gate to source capacitance, C_{gs}, and the gate to drain capacitance, C_{gd}. Continuing the above example, with C_{gs} = 1.5 pF and C_{gd} = 0, the three dB corner frequency is 4.3 GHz under matched conditions and 3.5 GHz with a VSWR of 1.5:1. Also, with C_{gs} = 0 and C_{gd} = .15 pF the corner frequencies become 9.0 GHz and 6.9 GHz, respectively. When both capacitances are considered at the same time, their interaction results in corner frequencies of 3.1 GHz and 2.5 GHz respectively. The output capacitance, C_{ds}, has a less significant effect at these frequencies but the drain resistance, R_{ds}, can reduce the effective load impedance and, therefore, reduce amplifier gain. Input and output match are also degraded under matched conditions but the output match can be improved when K > 1. As much as 3 dB of gain can be lost due to R_d, and once again the sensitivity depends on the amount of negative feedback applied.

The gain roll-off due to the parasitic capacitance of the FET is accompanied by a degradation of input VSWR. The output VSWR remains acceptable due to the effect of R_{ds}. Therefore, amplifier performance can be significantly enhanced by adding an input matching network to the amplifier as shown in Figure 2. It is essential to use a low pass matching structure to maintain acceptable low frequency performance. Standard tables can be used to determine the values of L and C once the effective input impedance is known, and computer optimization is used as the final design step to account for the remaining parasitic elements.

AMPLIFIER DESIGN

The design procedure described above was used to design a negative feedback amplifier to cover the 5 MHz to 2 GHz band. A 1200 micron wide FET consisting of four 300 micron wide fingers was selected to obtain a transconductance of 80 mS at low noise bias. The effective value of the feedback resistor was increased to 375 ohms to maintain a gain of at least 10 dB when the effects of bias networks and R_{ds} are considered. The feedback resistor, R_p, was split into four parallel resistors of 1500 ohms each and distributed between the four gate fingers to minimize parasitic inductance and capacitance. An alternate way of looking at the four gate fingers and their associated feedback resistors is as four separate feed-

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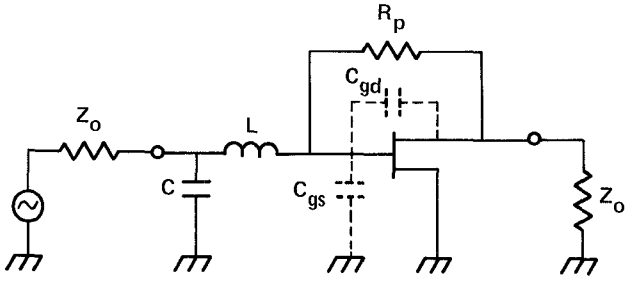

Figure 2 Feedback amplifier with low pass input matching network.

200 ohms, wired in parallel. The lumped element input matching network is placed at the 50 ohm side of the connection to conserve chip area and further reduce parasitic effects. With the FET parameters used above, C = 2 pF and L = 5 nH are needed to bring the input impedance back to 75 ohms (1.5:1 VSWR) at 2 GHz. After optimization across the DC to 2 GHz band with the simplified FET model, the element values become C = 1.4 pF and L = 5.3 nH. Further optimization including a full FET device model, parasitic interconnection and bias elements, and the higher value of R_p results in final matching element values of C ≅ 1.2 pF and L = 5.4 nH. The capacitor is implemented as a metal-insulator-metal parallel plate capacitor and the inductor is implemented as a spiral inductor to conserve chip area. With proper modeling of the parasitics, both function to at least 2 GHz. A full schematic of the amplifier and bias circuitry is shown in Figure 3.

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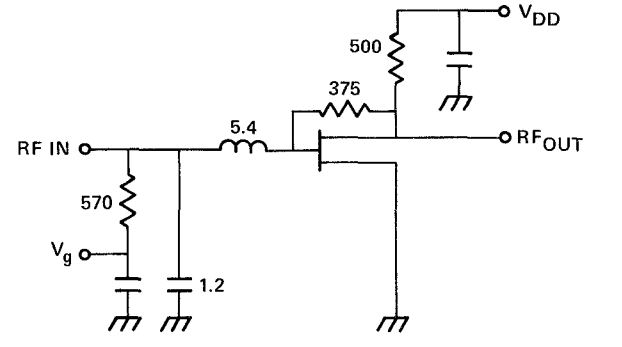

Figure 3 Feedback amplifier schematic.

FABRICATION

The design is implemented on a semi-insulating GaAs substrate containing lumped elements, ion implanted resistors, spiral inductors, MIM capacitors, and FETs. Both Cr doped and undoped S.I. substrates grown by the horizontal Bridgeman and the liquid encapsulated Czocharalski (LEC) techniques have been used for device fabrication. A preselection test for bulk S.I. GaAs

substrates involving qualification of the entire GaAs ingot by sampling the front and the tail of each boule is first employed to select the ingot to be used. The qualification procedure assesses the ability of the S.I. substrate to withstand high temperature (850°C) processing and to yield device quality active layers by ion implantation. Direct implantation of Si^+ in selected areas, defined photolighographically, is used for forming the FET and resistor active areas. The wafer is then coated with reactively sputtered Si_3N_4 and annealed at 850°C in an H_2 ambient resulting in active layers of ~ 1000 Ω/□ sheet resistivity and 4000-5000 $cm/^2$ V-sec Hall mobility at 1×10^{17} cm^{-3} doping concentration. AuGe/Ni is used to form the ohmic contacts. The 1 μm long gates and the first level metallization are defined by conventional photolithography and liftoff process. Gate metal is Ti/Pt/Au for good reliability. A dielectric layer of Si_3N_4 is used for the insulation between the first level and the second level interconnections and dielectric for the circuit MIM capacitors. Typically, 130 pF/mm^2 capacitance is obtained. Capacitance uniformity and reproducibility can generally be maintained to within ±5%. Reactive ion etching is used to open via holes in the dielectric wherever the first level metallization needs to be accessed. Second level metallization is gold plated to a thickness of 2-3 μm to reduce RF losses in the passive circuitry. The GaAs wafer is thinned to 125 μm and metallized on the back to complete the ground plane.

RESULTS

Figure 4 is a photograph of the 1.5 by 1.5 millimeter chip which is 125 microns thick. (The test structures at the bottom of the chip are not part of the amplifier circuitry.) Measured gain and noise figure are shown in Figure 5 when the amplifier is biased for low noise operation (V_{ds} = 2.6 volts, I_{ds} = 80 ma). Note that the gain peak at low frequency is due to the external bias networks (used for testing) and is not inherent in chip performance. A separate low frequency measurement at 5 MHz yielded a measured gain of 12 dB as indicated by the dot in Figure 5. Input match is excellent at 2 GHz but at low frequencies return loss is 7 dB due to the 375 ohm feedback resistor and a lower than expected transconductance at low noise bias. Output return loss is better than 12 dB across the band and is better than 16 dB below 1 GHz. When the amplifier is biased for maximum gain, the output match remains excellent and the input return loss is better than 10 dB across the band due to higher transconductance. Gain shape remains the same but the gain is increased by 1 dB. At this bias point saturated power in excess of +20 dBm is obtained across the band while +23 dBm is obtained below 1 GHz.

CONCLUSION

In conclusion, the application of negative resistive feedback around a 1200 micron wide GaAs FET has led to the fabrication of a low noise

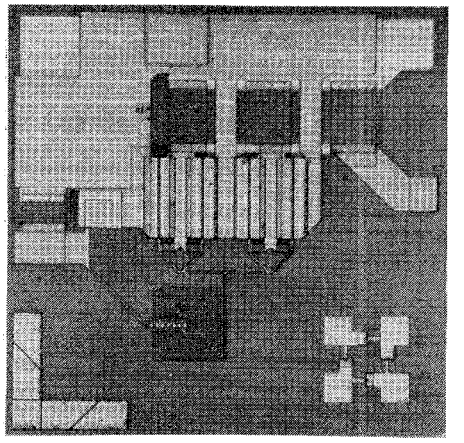

Figure 4 1.5 × 1.5 millimeter amplifier chip.

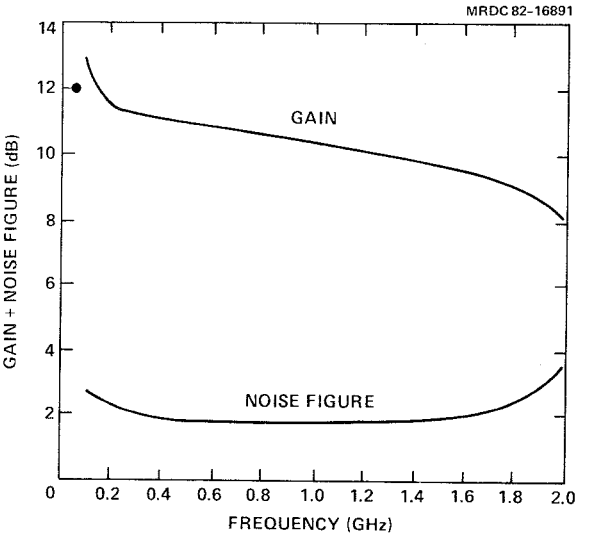

Figure 5 Measured gain and noise figure.

wideband amplifier suitable for use as a utility amplifier or an intermediate frequency (IF) amplifier. The high dynamic range amplifier is useful as both a discrete component and part of a larger monolithically integrated circuit. Potential future enhancements of the circuit include higher frequency performance, active loads for higher large signal efficiency, and a level shifting circuit to enable DC cascading of the amplifiers.

REFERENCES

1. H.P. Weidlich, J.A. Archer, E. Pettenpaul, F.A. Pety, and J. Huber, "A GaAs Monolithic Broadband Amplifier, ISSCC Digest of Technical Papers, pp. 192-193, Feb., 1981.